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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TRUNG T. DOAN,
RANDHIR P. S. THAKUR
and YAUH-CHING LIU

Appeal 2008-1034
Application 10/774,762
Technology Center 2800

Decided: May 2, 2008

Before PETER F. KRATZ, CATHERINE Q. TIMM, and LINDA M. GAUDETTE, *Administrative Patent Judges*.

TIMM, *Administrative Patent Judge*.

DECISION ON APPEAL

1Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 19-42. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

I. BACKGROUND

The invention relates to a semiconductor device with a number of layers. Claims 19, 26, 33, and 39 are illustrative of the subject matter on appeal:

19. A semiconductor device substantially impervious to the effects of buckling, said device comprising:

a) a single first planarization layer disposed on a semiconductor substrate, the single first planarization layer having a first reflow temperature and a first thermal coefficient of expansion;

b) a barrier film disposed on the single first planarization layer; and

c) a single second planarization layer disposed on the barrier film, the single second planarization layer having a second reflow temperature and a second thermal coefficient of expansion, wherein the barrier film does not reflow at the first or second reflow temperatures and retains its structural integrity to isolate the single first planarization layer from the single second planarization layer, thereby preventing the single first planarization layer and the single second planarization layer from interacting, and enabling the single first planarization layer and the single second planarization layer to uniformly reflow.

26. A planar multilayered semiconductor device comprising:

a substrate;

a first single flowable layer disposed on the substrate and having a thermal coefficient of expansion;

a nitride film disposed on the first layer; and

a second single flowable layer disposed on the nitride film, the second single flowable layer having another thermal coefficient of expansion, wherein the nitride film retains its structural integrity at the reflow

temperatures of the first single flowable layer and the second single flowable layer, thereby preventing the first single flowable layer and the second single flowable layer from interacting, and enabling the first single flowable layer and the second single flowable layer to uniformly reflow.

33. A multilayer heterostructure semiconductor device having a planar configuration comprising:

a semiconductor substrate;

a first single planarization layer disposed on the substrate, the single first planarization layer having a first thermal coefficient of expansion and a first reflow temperature;

a barrier film disposed on the single planarization layer, said barrier film having structural integrity; and

a single second layer disposed on the barrier film, wherein the barrier film prevents the single first planarization layer and the single second layer from interacting when the single first planarization layer is heated to a temperature above the first reflow temperature, the single second layer having a second thermal coefficient of expansion.

39. An apparatus, comprising:

a first layer at a temperature of at least 700ºC, the first layer being in a reflow state;

a second layer at the temperature of at least 700ºC, the second layer being in a reflow state;

a barrier layer at a temperature of at least 700ºC, the barrier layer being disposed between the first and second layers, wherein the barrier layer is not in a reflow state and maintains its structural integrity to isolate the first layer from the second layer.

Appellants request review of the two rejections maintained by the Examiner, namely, the rejection of claims 19-38 under 35 U.S.C. § 102(e) as anticipated by Woo et al. (US 5,262,352 issued Nov. 16, 1993); and the rejection of claims 39-42 under 35 U.S.C. § 103(a) as unpatentable over Woo in view of Cheung et al. (US 4,693,925 issued Sep. 15, 1987).

II. DISCUSSION

Appellants organize their arguments by issue (Br. 10-15). In arguing the issues, Appellants focus on the independent claims 19, 26, 33 and 39. Therefore, we decide the appeal on the basis of claims 19, 26, and 33 as to the first ground of rejection and on the basis of claim 39 as to the second ground of rejection.

A. *Anticipation by Woo*

Of the claims rejected as anticipated by Woo, claim 33 is the broadest in scope. With respect to claim 33, Appellants contend that: (1) the Examiner has misinterpreted the term "planarization layer," and Woo has no such layer (Br. 10-12); (2) Woo does not teach or suggest the combination of layers required by the claim (Br. 15); and (3) Woo does not disclose layers having different thermal coefficients of expansion or reflow temperatures (Reply Br. 3).

The Examiner contends the claim is drawn to a device and "planarization" amounts to an intended use or function which does not limit the structure of the layer (Ans. 10), and Woo discloses the combination of layers (Ans. 11).

Two issues of claim interpretation arise from the contentions of the Examiner and the Appellants: (1) what is the meaning of "planarization" in

the context of claim 33; and (2) does claim 33 require different thermal coefficients of expansion and reflow temperatures based on the language "first" and "second" used before those terms?

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027(Fed. Cir. 1997). Absent claim language carrying a narrow meaning, we only limit the claim based on the specification when those sources expressly disclaim the broader definition. *In re Bigio*, 381 F.3d 1320, 1324-25 (Fed. Cir. 2004).

Appellants point to no specific definitions or disclaimers of broad meaning in the Specification. We find the following discussions of planarization in the Specification.

> Previous methods used to ensure the wafer surface planarity have included forming an oxide such as BoroPhosphoSilicate Glass ("BPSG") layer on the wafer surface. These methods have then employed a heating step, as applied to the wafer, to reflow and planarize the oxide layer.

(Specification 1:14-18.)

> Another method which has been used to produce a planar wafer surface is to use the oxide reflow method described above, in conjunction with spin coating the wafer with photoresist. The spin coating fills the low points on the wafer surface, thereby producing a planar surface. Next, a dry etch, which removes photoresist and oxide at a rate sufficiently close to 1:1, etches

> the photoresist and the high points on the wafer surface, thereby producing a planar oxide layer on the wafer surface.

(Specification 2:23 to 3:4.)

> The first step of the present method involves forming a planarization layer superjacent a semiconductor substrate. The planarization layer comprises tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") or tetraethylorthosilicate ("TEOS").

(Specification 4:11-17.)

> Finally, the substrate is heated sufficiently to at least a temperature of approximately 700 °C to cause the planarization layer to expand according to a first thermal coefficient of expansion, the second layer to expand according to a second thermal coefficient of expansion, and the structural integrity of the barrier film to be maintained. This results in the barrier film isolating the planarization layer from the second layer, thereby preventing the planarization layer and the second layer from interacting during the heating step. Further, it enables the planarization layer to go through a solid state reaction and the second layer to obtain a uniform reflow.

(Specification 4:29 to 5:10.)

From the above descriptions in the Specification, we determine that "planarization" as used in the claims to describe a layer would have been understood by those of ordinary skill in the art as referring to a layer that has capability of providing a planar surface on the semiconductor substrate. Within the claim, "planarization" has a functional meaning. Moreover, as pointed out by the Examiner, the claim is directed to a device. A device must be distinguished structurally from the prior art. We agree with the Examiner that the function of the layer is limiting only in so far as it serves

to structurally distinguish the claimed device from devices in the prior art. While a patent applicant is free to recite features of a product or apparatus functionally, doing so carries with it a risk. As stated in *In re Swinehart*, 439 F.2d 210, 212 (CCPA 1971) as reproduced in *In re Schreiber*, 128 F.3d 1473, 1478 (Fed. Cir. 1997):

> where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on.

In the present case, it is reasonable to conclude that the layer 14 of Woo inherently has the structure of a "planarization layer." The layer is formed from a conductive material which could be subject to reflow (Woo, col. 3, ll. 49-52) or could be made planar by other methods. The burden has shifted to Appellants to show that, in fact, the layer 14 of Woo would not inherently be capable of performing the function of planarization. Appellants have not provided persuasive evidence that the conductive layer 14 would not be so capable.

Turning to the question of whether claim 33 requires different thermal coefficients of expansion and reflow temperatures based on the language "first" and "second" used before those terms, we determine that it does not. As a first matter, claim 33 does not require the second layer have any reflow temperature. While claim 33 does require the first planarization layer have a first thermal coefficient of expansion and the second layer have a second thermal coefficient of expansion, the words "first" and "second," broadly, but reasonably interpreted, simply require that the layers each have some

thermal coefficient of expansion. We cannot say that the words "first" and "second" necessarily require that the thermal coefficients of expansion be different from each other. Nothing in the Specification limits those words to the narrower meaning and the claim does not say that the values must be "different."

Appellants have not convinced us of a reversible error on the part of the Examiner in terms of the finding that Woo describes a first planarization layer having a first thermal coefficient of expansion and a first reflow temperature as well as a second layer with a second coefficient of thermal expansion.

The last question is whether Woo describes the combination of layers required by claim 33. Appellants contend that Woo fails to disclose how to select from among the lists materials disclosed for each of the layer such that the combination of layers recited by the claim arises. However, Appellants have not specifically pointed out what selection is required to meet the requirements of claim 33. The Examiner finds that Woo describes layers meeting the requirements of the planarization layer (layers 14 and/or 15), barrier film (layer 16), and second layer of the claim (layers 17 and/or 18 and/or 18) (Ans. 4). Layer 14 is conductive and made of materials that would have a thermal coefficient of expansion and a reflow temperature (metals, metal alloys, etc.). Layer 16 overlies the layers 14 and 15 and would be capable of functioning in accordance with the claimed barrier function based on its position and structure. Moreover, the second layer (layers 17 and/or 18 and/or 20) is disposed on the barrier film and would inherently have a coefficient of thermal expansion. No particular selection of materials is required to meet the requirements of claim 33.

Appellants have not convinced us of a reversible error in the Examiner's rejection of claim 33. Claims 34-38 depend from claim 33 and are not separately argued. Therefore, we sustain the rejection of claims 33-38 as anticipated by Woo.

With respect to claims 19 and 26, Appellants also contend that Woo does not describe the claimed combination of layers (Br. 15). For instance, with regard to claim 19, Appellants point out that this claim requires a barrier film that "does not reflow at the first or second reflow temperatures" (Br. 15). The Examiner contends that Woo discloses the combination of layers recited, arguing that patentability does not depend on the method of production (Ans. 11).

The language "does not reflow at the first or second reflow temperatures" serves to limit the scope of materials that can serve as the barrier film: that film must have a reflow temperature less than the reflow temperatures of the first planarization layer material and the second planarization material. The Examiner has not provided sufficient evidence that the genus of materials for the layer relied upon as the barrier layer, i.e., dielectric layer 16, would necessarily have the required reflow property. While it is possible that some of the materials might have the required property when selected for use in combination with other specific materials for the other layers, picking and choosing from amongst the layer materials would be required. This type of picking and choosing, while appropriate in an obviousness determination, has no place in an anticipation rejection. "[R]ejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in 'the prior art.'" *In re Arkley*, 455 F.2d 586, 587 (CCPA 1972).

With respect to claim 26, this claim requires a nitride film sandwiched between first and second single flowable layers. This nitride layer must retain its structural integrity at the reflow temperatures of the first and second reflowable layers, thereby preventing the first single flowable layer and the second single flowable layer from interacting, and must enable the first single flowable layer and the second single flowable layer to uniformly flow. For the nitride layer, the Examiner relies upon the dielectric layer 16 of Woo. Woo describes several nitrides for layer 16, including silicon nitride, oxide-nitride-oxide (ONO), oxynitride materials, and plasma enhanced silicon nitride. In order to meet the terms of the claim, one must select one of these nitrides for layer 16 and then select one of the conductive materials listed for layers 14 and/or 15 and also select one of the materials listed for layers 17 and/or 18 and/or 20 such that the layers have the properties required by the claim. The descriptions of the materials within Woo are not specific enough to support a reasonable conclusion that the properties will be inherently possessed without improper picking and choosing among the materials. Woo discloses a preference for doped polysilicon for layers 14 and 18, but the Examiner has not provided any reasonable basis to believe that these doped polysilicons necessarily have the required properties.

Because the Examiner did not establish anticipation with regard to claims 19 and 26, we do not sustain the rejection of claims 19-32 as anticipated by Woo.[1]

[1] We acknowledge Appellants' reliance on Silicon Processing for the VLSI Era (Wolf) in their arguments. A copy of this evidence was provided in the Evidence Appendix, but the evidence had not been previously before the Examiner (Br. 14). The Examiner has not indicated that the evidence is entered, or otherwise discussed Wolf. Accordingly, we do not consider this

B. *Obviousness over Woo and Cheung*

The Examiner rejected claims 39-42 under 35 U.S.C. § 103(a) as unpatentable over Woo in view of Cheung. Claim 39 requires first and second layers in a reflow state and a barrier layer not in a reflow state.

The Examiner relies upon Woo in the same capacity as above and further finds that Woo describes depositing a polysilicon interconnection layer(24) and siliciding that layer (Ans. 8). The Examiner further finds that Cheung describes siliciding by depositing refractory metal on polysilicon and annealing at 600-800 °C. The Examiner concludes that it would have been obvious for one of ordinary skill in the art to silicide the layers of Woo as taught by Cheung, annealing to 700 °C or greater (Ans. 8).

Appellants point out that Woo does not disclose that any of the layers are in a reflow state and Cheung teaches applying a heat pulse of 600-800 °C for 10-20 seconds to permit a "reaction to occur forming the metal silicide." (Br. 18 citing Cheung, col. 3, ll. 45-50). According to Appellants, the Examiner has not identified any layer in a reflow state.

The Examiner does not address the portion of Cheung pointed out by Appellants.

The issue is: It is reasonable to conclude that applying a heat pulse as directed by Cheung in the siliciding step of Woo would necessarily result in reflowing the first and second layers of Woo (layers 14 and/or 15 and layers 17 and/or 18 and/or 20)? We answer this question in the negative.

We cannot say that the Examiner has provided enough evidence to show that siliciding with a 10 to 20 second pulse of 600-800°C heat would

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evidence. See 37 C.F.R. § 41.33(d)(2).

necessarily cause the first and second layers of Woo to reflow. As pointed out by Appellants, the heating is for a different purpose (siliciding) and is applied for a short amount of time. The evidence simply does not adequately support the Examiner's determination.

We do not sustain the rejection of claims 39-42 under 35 U.S.C. § 103(a) as unpatentable over Woo in view of Cheung.

III. CONCLUSION

We sustain the rejection of claims 33-38 under 35 U.S.C. § 102(e), but do not sustain the rejection of claims 19-32 on that ground. We do not sustain the rejection of claims 39-42 under 35 U.S.C. § 103(a).

IV. DECISION

The decision of the Examiner is affirmed-in-part.

V. TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal maybe extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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